Remarks

Claim 19, 25, 28 and 35 have been amended. No claims have been canceled. Therefore, claims 19-35 are now presented for examination.

Claims 19, 21, 25-26, 28, 30 and 35 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng (U.S. Patent No. 5,694,581) and Jones et al. (U.S. Patent No. 5,619,723) and further in view of Thompson et al. (U.S. Patent No. 6,341,342). Applicant submits that the present claims are patentable over any combination of Cheng, Jones and Thompson.

Claim 19 recites:

> A system comprising:
> a Basic Input/Output System (BIOS);
> a system bus coupled to said BIOS;
> an integrated drive electronics (IDE) interface coupled to said system bus that communicates directly with said BIOS via said system bus;
> a striping controller coupled to said IDE interface;
> a first disk drive including first IDE electronics, said striping controller coupled to said first IDE electronics;
> a second disk drive including second IDE electronics, said striping controller coupled to said second IDE electronics, said first and said second IDE electronics each having data separator electronics, data formatting electronics and head positioning electronics; and
> said striping controller causes data being transmitted between said interface and said first and second drives to be written to and read from the first and second drives in an interleaved form and substantially in parallel.

In the Advisory Action dated September 12, 2003, the Examiner has indicated that the prior art of record does not teach or suggest a bus interface that communicates directly with BIOS. Therefore, claim 19 is patentable over Cheng and Jones in view of Thompson. Claims 20-24 depend from claim 19 and include additional limitations. As a

result, claims 20-24 are also patentable over the combination of Cheng, Jones and Thompson.

Claim 25 recites:

> A method comprising:
> transmitting an integrated drive electronics (IDE) request from a Basic Input/ Output System (BIOS) onto a system bus;
> receiving said IDE request at an IDE interface connected to said system bus, said interface communicating directly with said BIOS;
> transmitting said IDE request to a striping controller coupled to said IDE interface and first IDE electronics of a first disk drive and second IDE electronics of a second disk drive;
> writing to and reading from the first disk drive and the second disk drive in an interleaved form and substantially in parallel in response to said IDE request.

Therefore, for the reasons stated above with respect to claim 19, claim 25 is also patentable over the combination of Cheng, Jones and Thompson. Since claims 26 and 27 depend from claim 25 and include additional limitations, claims 26 and 27 are also patentable over the combination of Cheng, Jones and Thompson.

Claim 28 recites:

> A striping disk controller comprising:
> an integrated drive electronics (IDE) interface coupled to a system bus that communicates directly with a Basic Input/ Output System (BIOS) separately coupled to said system bus; and
> control logic coupled to the IDE interface and first disk electronics of a first disk drive and second disk electronics of a second disk drive, the control logic to cause data being transmitted via the system bus to be written to and read from a first disk drive and a second disk drive in an interleaved form and substantially in parallel.

Thus, for the reasons stated above with respect to claim 19, claim 28 is also patentable over the combination of Cheng, Jones and Thompson. Since claims 29-34

depend from claim 28 and include additional limitations, claims 29-34 are also patentable over the combination of Cheng, Jones and Thompson.

Claim 35 recites

> A system comprising:
> a central processing unit (CPU) that executes an operating system including a Basic Input/Output Operating System (BIOS);
> a system bus coupled to the CPU;
> an IDE interface coupled to the system bus that communicates directly with the BIOS via the system bus;
> a striping controller coupled to the IDE interface;
> a first storage device, including first IDE electronics, said striping controller coupled to said first IDE electronics; and
> a second storage device, including second IDE electronics, said striping controller coupled to said second IDE electronics;
> the striping controller, based on a standard IDE driver instruction, causes data being received to be written to and read from the first and second storage devices in an interleaved form and substantially in parallel.

Thus, for the reasons stated above with respect to claim 19, claim 35 is also patentable over the combination of Cheng, Jones and Thompson. Since claims 36 and 37 depend from claim 35 and include additional limitations, claims 36 and 37 are also patentable over the combination of Cheng, Jones and Thompson.

Claims 20, 22, 27, 29, 31, 34 and 36 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng (U.S. Patent No. 5,694,581) and Jones et al. (U.S. Patent No. 5,619,723) and Thompson et al. (U.S. Patent No. 6,341,342) in further view of Anderson (U.S. Patent No. 5,905,910). As discussed above, the Examiner has stated that the prior art of record does not teach or suggest a bus interface that communicates directly with BIOS. Accordingly applicant submits that the present claims are patentable over any combination of Cheng, Jones, Thompson and Anderson.

Claims 23, 24, 32 and 33 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng (U.S. Patent No. 5,694,581) and Jones et al. (U.S. Patent No. 5,619,723) and further in view of Jenkins et al. (U.S. Patent No. 4,047,157). As described above, the Examiner has indicated that the prior art of record does not teach or suggest a bus interface that communicates directly with BIOS. Therefore, the present claims are patentable over the combination of Cheng, Jones, Thompson and Jenkins.

Claim 37 stands rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng (U.S. Patent No. 5,694,581) and Jones et al. (U.S. Patent No. 5,619,723) and Thompson et al. (U.S. Patent No. 6,341,342) in further view of further in view of Mizuno et al. (U.S. Patent No. 5,608,891). As previously discussed, the Examiner has asserted that the prior art of record does not teach or suggest a bus interface that communicates directly with BIOS. Therefore, the present claims are patentable over the combination of Cheng, Jones, Thompson and Mizuno.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: September 22, 2003

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